

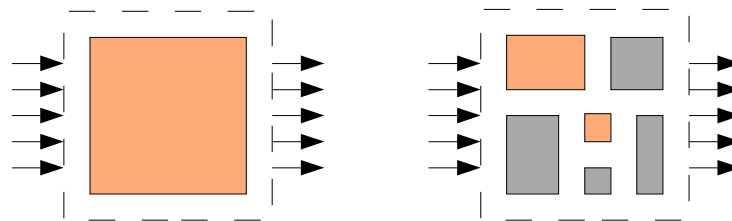
ART

Dynamically Reconfigurable Logic IP

Overview

ART is a dynamically-reconfigurable logic technology designed to implement digital signal processing functions. ART brings the flexibility of a conventional DSP core, with the size and power consumption of “hard-wired” RTL design.

ART is delivered as IP, allowing anything from an entire ASIC to a part of an SoC or ASSP to benefit from the flexibility and reconfigurability enabled by ART.



ART can be used for a whole chip, or parts of a chip

Advantages of ART

ART brings major advantages to a chip manufacturer when compared to traditional RTL-based design or DSP-based devices:

- Reduced risk – designs can be modified after tape-out, without requiring new silicon
- Speed of design – ART-based design is faster than RTL-based design
- Low area and power cost – designs are similar to hard-wired silicon in area and power

ART features

- Process-independent
 - Works with any process which supports standard Verilog synthesis flow
- Automatic memory generation
 - Optimised interface to silicon and FPGA memory generators
 - Memory instancing is simple and automatic
- Automatic support for FPGA-based verification
 - ART tools support FPGA-based targets with no need for code modification
- Advanced power optimisation
 - ART devices automatically include clock gating which allows parts of a device to be stopped when not in use
- True dynamic reconfiguration
 - ART-based devices can be reconfigured every clock cycle – allowing unprecedented levels of hardware reuse
- Fast SystemC simulation model
 - ART tools generate SystemC hardware model for firmware development

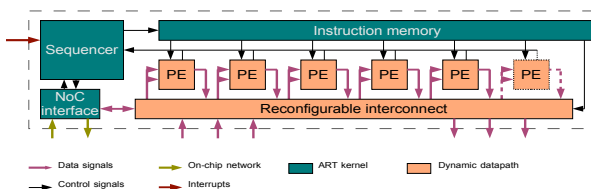
ART performance

ART is highly scalable, capable of providing processing from a few MOPS to tens of GOPS at typical clock speeds of 100MHz to 500MHz¹.

It should be noted that the inherent support for parallelism and highly flexible memory architectures in ART mean that ART is able to achieve much higher OPS/MHz values than other technologies and so is able to run at significantly lower clock speeds for the same computing performance.

ART structure

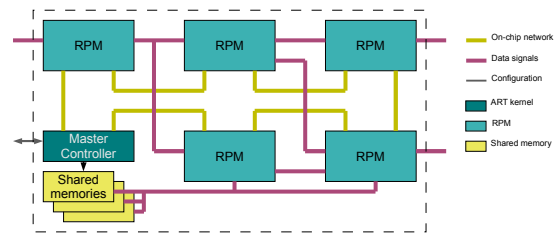
The basic processing block of an ART device is a “Reconfigurable Processing Matrix” (RPM) as shown below.



An RPM consists of a dynamically reconfigurable datapath made up of design-time selected Processing Elements (PEs) which are connected together by a Reconfigurable Interconnect (RI). A program (known as a “sequence”) running on the Interconnect Sequencer (ISEQ) in the RPM determines the connections between PEs and the operation of each PE (e.g. whether an adder/subtractor adds or subtracts or whether a register is loaded) on every clock cycle. The entire configuration of the datapath in an RPM can change each clock cycle under control of the sequence.

Two or more RPMs can be connected together to form an “ART Core” as shown below.

The RPMs are connected together and to a Master Controller via a high-speed token ring network-on-chip. This is used both for configuration of the Core, and for communication between RPMs when the device is operating.



The Master Controller also controls access to Shared Memories which can be used for communication between RPMs. In addition to the network-on-chip and Shared Memories, RPMs can be connected together using Direct Interconnect (DI) which provides dedicated point-to-point links between RPMs.

ART PE library

ART's library of Processing Element (PE) “building blocks” is extensive and includes the following (among others):

- pe_addsub
- pe_barrel_shifter
- pe_bitwise_multifunction
- pe_comparator
- pe_counter
- pe_crc
- pe_decode
- pe_edge_detect
- pe_fifo_controller_async
- pe_fifo_controller_sync
- pe_fsm_4state
- pe_mailbox
- pe_memory_1port
- pe_memory_2port
- pe_multiplier
- pe_multiply_accumulate
- pe_priority_encode
- pe_reduce_any_3to1
- pe_reg_file_2port
- pe_reg_file_4port
- pe_register
- pe_round_saturate
- pe_shift_register
- pe_sign_extend

ART design flow

ART divides the design process into two separate stages:

1. Datapath design
 - The dynamic datapath is created using Aky's ART Architecture Definition language (AAD)
 - The ART Architecture Compiler (artac) and supporting tools turn the

¹ Maximum clock speed depends on underlying silicon and memory technology.

AAD description into fully synthesisable Verilog and SystemC models, and create all required memory instances for the target technology

2. Control implementation

- The control aspects of the design are coded in firmware using ART Assembly Language (AAL)
- The ART Assembler (artasm) and supporting tools turn the AAL into a configuration bitstream which is loaded into the ART device at power-on

The separation of the design of datapath and control allows a substantial increase in designer productivity, and a reduction in errors. In addition, the fact that the control element of the design is embodied in firmware which can be changed after the device is manufactured means that even bugs missed during verification are very likely to be fixable without needing a re-spin of silicon.

Supported technologies

The ART design tools can produce Verilog for synthesis using standard cell libraries, Verilog for synthesis to FPGA or SystemC for simulation.

The designer never needs to make any changes to the input code in order to move a design from one supported technology to another – all required changes are performed automatically by the ART design tools. In order to support this “process independence”, ART uses an abstract memory model where memories are specified as simply single- or dual-ported, can be of any size (width and depth), and may or may not have “lanes” (allowing writes to affect only part of a word). The ART design tools understand the memories supported by the targeted technology and automatically build physical memories which match the specified memory – possibly by connecting together several physical memories of differing sizes in order to create a memory of the size and characteristics specified in the design.

Currently, the ART design tools support the following technologies:

Standard cell:

- Artisan for TSMC 0.18µm
- Artisan for TSMC 0.15µm
- Artisan for TSMC 0.13µm
- Artisan for TSMC 90nm

FPGA:

- Altera Stratix II & III
- Xilinx Virtex 4
- Xilinx Spartan 3

The ART design tools use a database which describes the memory capabilities of various implementation technologies. This allows support for new technologies to be added easily and quickly by Akya (typically within one day of receiving the details of the supported memories).

Applications for ART

ART is suited to any application which requires devices to be reconfigurable. The degree of reconfigurability depends on the decisions made when the device is designed and can range from a limited amount such as the ability to change the function of an interface on an SoC to support different standards to a highly reconfigurable solution similar in flexibility to a general-purpose CPU or DSP chip.

ART offers advantages in many applications including:

- Fast-moving consumer goods
 - ability to support multiple product variants with single silicon design
 - field upgrades for bug-fixes and new features
 - silicon area savings as multiple standards share silicon resources
- Support of evolving standards
 - pre-standard equipment can be fixed by a firmware upgrade when the standard is finalised

- evolving technologies – e.g. airport security scanners
- Telecoms infrastructure
 - mobile telephone basestations
- Low-power, flexible devices
 - portable multimedia devices
 - mobile telephones
 - radios and multimedia
 - automotive
 - Multimedia and driving aids
 - GPS
 - Battery-powered medical devices
- Low-volume devices
 - several variants of a low-volume device may be combined into a single device (with variants differentiated by reconfiguration), with increased production run size making silicon implementation financially viable
- Customisable ASSP
 - ASSP manufacturers can ship parts with significant ART-based

computing resources available at key points in datapaths within the ASSP, thereby allowing their customers to modify the function of the ASSP by implementing their own algorithms and/or modifications to the existing algorithms

- End-product function flexibility
 - a single device can support multiple end-product variants
 - costs can be further reduced by (for example) speed-grading manufactured parts, and running more complex algorithms on high-speed parts in high-end products, and lower-complexity algorithms on low-speed parts in entry-level products.

High-level language design

Akya is working with Cadence to adopt a complete high-level synthesis design route for ART based around Cadence's C to Silicon tool and the TLM-driven design flow.

Akya is also working to produce stand-alone C compilers for ART RPMs.

Summary

ART is a combination of IP and EDA which allows the design of reconfigurable devices which have power and area similar to that of hard-wired RTL-based devices. ART reduces risk in the design of modern integrated circuits. ART is a new approach to logic design which offers radical performance improvements over existing methods.

Contact

Akya Limited, Corunna House, 42-44 Ousegate, Selby YO8 4NH, United Kingdom

Tel: +44 (0) 1757 292626 (UK)
+1 650 207-7900 (US)
+81 427 561041 (Japan)

Email: enquiries@akya.co.uk (English)
enquiries-jp@akya.co.uk (Japanese)

This document is copyright © 2010, Akya (Holdings) Limited. All rights reserved.
The technology and computer programs described are proprietary and protected by patents, patents pending and copyright. No license is granted or implied by this document.